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lmid.* connected to a corresponding write driver 200, 210 and sense amplifier 300, 310. The source terminals of the memory cell transistors in the cell block 101 are connected to one source line SL to thereby be driven by the source line driver 500.

IN THE DRAWINGS

Please replace old FIG. 3 with new FIG. 3. A redline version of the drawing showing the changes is included herewith.